WT32-S3-WROVER1

WT32-S3-WROVER2

Datasheet

2.4GHz WIFi(802.11b/g/n) and Buletooth 5(LE) module

Built around ESP32-S3 series of SoCs,Xtensa dual-core 32-bit LX7 microprocessor

Flash up to 16 MB,PSRAM up to 8MB

On-board PCB antenna or external antenna connector

V1.0.0

Sept 16, 2021

Wireless-Tag Technology Co., Ltd

About this document

This document provides users with the technical specifications for WT32-S3-WROVER1 and WT32-S3-WROVER2.

Document updates

Please visit Wireless-Tag's official website to download the latest version of the document.

Revision history

Please go to the document revision history page to view the revisions of the document.

Revision History

No.	Version	Changes	Change (+/-) Descriptions	Author	Date
1	V1.0.0	C	First release	Fiona	Sept 16, 2021

*Changes：C——create, A——add, M——modify, D——delete

Contents

1 Module Overview

1.1 Features

MCU

- ESP32-S3 series of SoCs embedded,Xtensa® dual-core 32-bit LX7 microprocessor, up to 240MHz
  - SRAM 512KB
  - RTC SRAM 16KB
  - ROM 384KB
  - Up to 8 MB PSRAM

WIFI

- IEEE 802.11b/g/n protocol
- Bit rate:802.11n uo to 150Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412~2484 MHz

Bluetooth

- Bluetooth LE:Bluetooth5,Bluetooth mesh
- 2Mbps PHY
- Long range mode
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2

Hardware

- Module interface: GPIO, SPI, LCD interface, UART, I2C, I2S, Camera interface, infrared remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SDIO host interface, GDMA, TWAI® Controller (ISO 11898-1 Compliant), ADC, Touch Sensor, Temperature Sensor, Timer and Watchdog
- 40MHz crystal oscillator
- Up to 16 MB SPI flash
- 8 MB PSRAM

- Operating voltage/Power supply: 3.0~3.6 V
- Operating ambient temperature: -40~85℃
- Package size: (18 × 31 × 3.3) mm

1.2 Description

WT32-S3-WROVER1 and WT32-S3-WROVER2 are two general-purpose Wi-Fi+Bluetooth low energy MCU modules, equipped with ESP32-S3 series chips. In addition to rich peripheral interfaces, the module also has powerful neural network computing capabilities and signal processing capabilities, which are suitable for various application scenarios in the AIoT field, such as wake word detection and voice command recognition, face detection and recognition, intelligent Home, smart home appliances, smart control panels, smart speakers, etc.

WT32-S3-WROVER1 adopts PCB onboard antenna, WT32-S3-WROVER2 adopts connector to connect external antenna.equipped with 4 MB SPI flash and 8 MB SPI PSRAM.

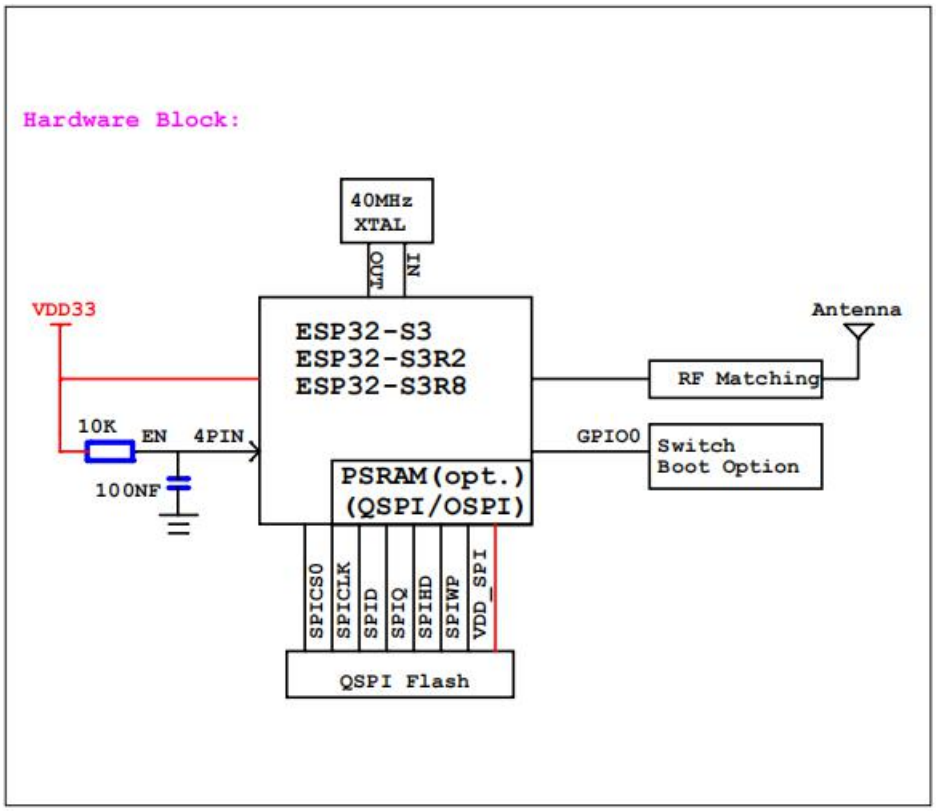
WT32-S3-WROVER1 and WT32-S3-WROVER2 uses ESP32-S3 chip. The ESP32-S3 chip is powered by an Xtensa® 32-bit LX7 dual-core processor that operates at up to 240 MHz. The user can power down the CPU and use the low-power coprocessor to monitor the state changes of peripherals or whether certain analog quantities exceed thresholds. ESP32-S3 also integrates rich peripherals, including SPI, LCD interface, UART, I2C, I2S, Camera interface, infrared remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SDIO host Interface, GDMA, TWAI® controller (ISO 11898-1 compliant), ADC, touch sensor, temperature sensor, timer and watchdog.

1.3 Applications

- Generic low-power IoT sensor hub
- Generic low-power IoT data logger
- Camera video streaming
- OTT TV box/set-top box equipment
- USB device
- Voice recognition
- Image recognition
- Mesh network
- Home automation
- Smart home control panel
- Smart buildings
- Industrial Automation
- Smart agriculture
- Audio equipment
- Health/Medical/Nursing
- Wi-Fi toys
- Wearable electronic products
- Retail & Catering
- Smart POS application
- Smart door lock

2 Block Diagram

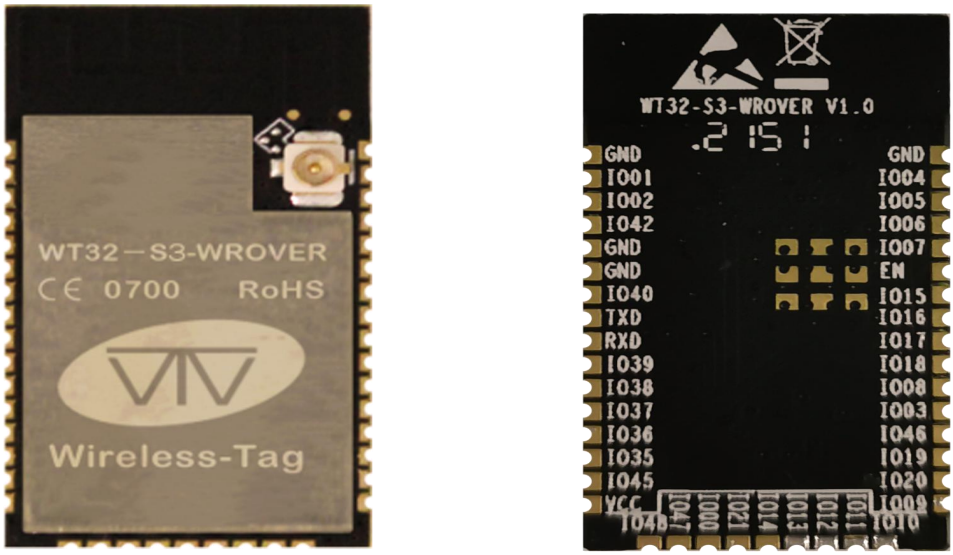
Figure 1 Block Diagram



3 Pin Definitions

3.1 Pin Layout

Figure 2 Pin Layout



3.2 Pin description

Table 1 Pin Definitions and Descriptions

Pin	Name	Description
1	GND	Ground
2	GPIO4	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
3	GPIO5	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
4	GPIO6	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
5	GPIO7	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
6	EN	Chip Enable pin: High level: on, enables the chip. Low level: off, the chip powers off, low current. Note: Do not leave the EN pin floating.
7	GPIO15	RTC_GPIO15,GPIO15,U0RTS,ADC2_CH4,XTAL_32K_P
8	GPIO16	RTC_GPIO16,GPIO16,U0RTS,ADC2_CH5,XTAL_32K_N
9	GPIO17	RTC_GPIO17,GPIO17,U1TXD,ADC2_CH6
10	GPIO18	RTC_GPIO17,GPIO17,U1TXD,ADC2_CH7,CLK_OUT3
11	GPIO8	RTC_GPIO8,GPIO8,TOUCH8,ADC1_CH7,SUBSPICS1

Pin	Name	Description
12	GPIO3	RTC_GPIO3,GPIO3,TOUCH3,ADC1_CH2
13	GPIO46	GPIO46
14	GPIO19	RTC_GPIO19,GPIO19,U1RTS,ADC2_CH8,CLK_OUT2,USB_D-
15	GPIO20	RTC_GPIO20,GPIO20,U1RTS,ADC2_CH9,CLK_OUT1,USB_D+
16	GPIO9	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
17	GPIO10	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
18	GPIO11	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
19	GPIO12	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
20	GPIO13	RTC_GPIO13,GPIO13,TOUCH13,ADC2_CH2,FSPIQ,FSPIIO7, SUBSPIQ
21	GPIO14	RTC_GPIO14,GPIO14,TOUCH14,ADC2_CH3,FSPIWP,FSPIDQS, SUBSPIWP
22	GPIO21	RTC_GPIO21,GPIO21
23	GPIO0	RTC_GPIO0,GPIO0
24	GPIO47	SPICLK_P_DIFF, GPIO47, SUBSPICLK_P_DIFF
25	GPIO48	SPICLK_N_DIFF, GPIO48, SUBSPICLK_N_DIFF
26	VCC	Power supply
27	GPIO45	GPIO45
28	GPIO35	SPIIO6, GPIO35, FSPID, SUBSPID
29	GPIO36	SPIIO7, GPIO36, FSPICLK, SUBSPICLK
30	GPIO37	SPIDQS, GPIO37, FSPIQ, SUBSPIQ
31	GPIO38	GPIO38, FSPIWP, SUBSPIWP
32	GPIO39	MTCK, GPIO39, CLK_OUT3, SUBSPICS1
33	U0RXD	U0RXD, GPIO44, CLK_OUT2
34	U0TXD	U0TXD, GPIO43, CLK_OUT1
35	GPIO40	MTDO, GPIO40, CLK_OUT2
36	GND	Ground
37	GPIO41	MTDI, GPIO41, CLK_OUT1
38	GPIO42	MTMS, GPIO42
39	GPIO2	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
40	GPIO1	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
41	GND	Ground

3.3 Strapping Pins

ESP32-S3 series has four strapping pins.

- GPIO0 = IO0
- GPIO45 = IO45
- GPIO46 = IO46
- GPIO3=IO3

Software can read the strapping values of these pins in the register "GPIO_STRAPPING". During the system reset of the chip (power-on reset, RTC watchdog reset, brown-out reset, analog super watchdog reset, crystal oscillator clock glitch detection reset), the Strapping pin has the same function as the one on its own pin. The level is sampled and stored in the latch, and the latch value is "0" or "1" and remains until the chip is powered off or turned off.

IO0, IO45, IO46 are connected to internal weak pull-up/pull-down by default. If these pins are not externally connected or the connected external lines are in a high impedance state, the internal weak pull-up/pull-down will determine the default value of the input level of these pins.

GPIO3 is in a floating state by default. The strapping value of GPIO3 can be used to switch the source of the JTAG signal inside the CPU, as shown in Figure 4. In this case, the strapping value is controlled by the external line, and the external line cannot be in a high impedance state. Table 3 lists all configuration combinations of EFUSE_DIS_USB_JTAG, EFUSE_DIS_PAD_JTAG and EFUSE_STRAP_JTAG_SEL to select the JTAG signal source.

Table 2 Strapping Pins

EFUSE_STRAP_JTAG_SEL	EFUSE_DIS_USB_JTAG	EFUSE_DIS_PAD_JTAG	JTAG Signal Source
1	0	0	Refer to Table 3
0	0	0	USB Serial/JTAG controller
Don’t care	0	1	USB Serial/JTAG controller
Don’t care	1	0	On-chip JTAG pins
Don’t care	1	1	N/A

To change the value of the strapping, the user can apply an external pull-down/pull-up resistor, or use the GPIO of the host MCU to control the strapping pin level when the ESP32-S3 is powered on reset.

After the reset is released, the strapping pins have the same functions as normal pins.

Please refer to Table 3 for the detailed boot modes for configuring the strapping pins.

Table 3Strapping pins

VDD_SPI Voltage [1]			
Pin	Default	3.3 V	1.8 V
IO45 [2]	Pull-down	0	1
Booting Mode [2]			

Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Dot'	0
Enabling/Disabling ROM Messages Print During Booting [3][4]			
Pin	Default	Enabled	Disabled
IO46	Pull-down	See the fourth note	See the fourth note
JTAG Signal Selection			
Pin	Default	EFUSE_DIS_USB_JTAG=0,EFUSE_DIS_PAD_JTAG=0, EFUSE_STRAP_JTAG_SEL=1	
GPIO3	N/A	0:JTAG signal from on-chip JTAG pins 1:JTAG signal from USB Serial/JTAG controller	

Note:

1. The VDD_SPI voltage is determined by the strapping value of GPIO45 or VDD_SPI_TIEH in eFuse. EFUSE_VDD_SPI_FORCE selection decision method in eFuse: 0: Determined by the strapping value of GPIO45; 1: Determined by EFUSE_VDD_SPI_TIEH in eFuse.
2. GPIO 46 = 1 and GPIO0 = 0 cannot be used.
3. The ROM Code is powered on and printed by default through the U0TXD pin, which can be switched to the GPIO17 (U1TXD) pin by the eFuse bit EFUSE_UART_PRINT_CHANNEL.
4.When both EFUSE_DIS_USB_SERIAL_JTAG and EFUSE_DIS_USB_OTG are 0, ROM boot messages will be printed to the USB Serial/JTAG controller. Otherwise, the messages will be printed to UART, controlled by GPIO46 and EFUSE_UART_PRINT_CONTROL. Specifically, when EFUSE_UART_PRINT_CONTROL value is:

0, print is normal during boot and not controlled by GPIO46.
1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
3, print is disabled and not controlled by GPIO46.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	-0.3	3.6	V
TSTORE	Storage temperature	-40	85	℃

4.2 Recommended Operating Conditions

Table 5 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T	Ambient temperature	-40	—	85	℃
Humidity	Humidity condition	—	85	—	%RH

4.3 Current Consumption Characteristics

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to the tables below.

Table 6 Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active(RF working)	TX	802.11b, 1Mbps, @20.5dBm	355
		802.11g, 54Mbps, @18dBm	297
		802.11n, HT20, MCS7, @17dBm	286
		802.11n, HT40, MCS7, @17dBm	285
	RX	802.11b/g/n, HT20	95
		802.11n, HT40	97

Note:

1. The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.

2. The current consumption figures in RX mode are for cases when the peripherals are disabled and the CPU is idle.

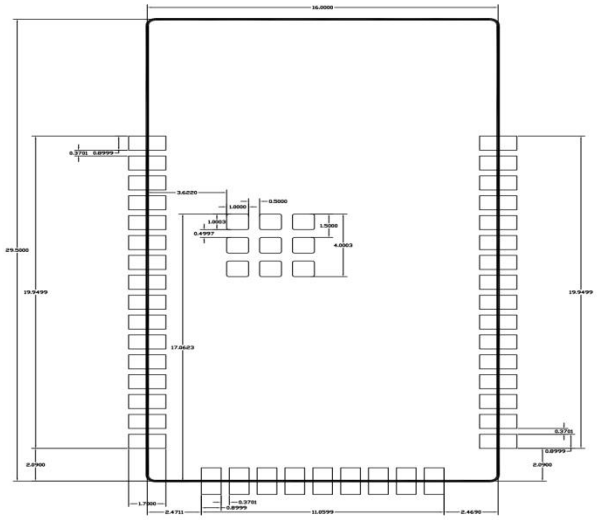
Table 7 Current Consumption Depending on Work Modes

Work mode	Description	Typ	Unit
Light-sleep	—	240	μA
Deep-sleep	RTC memory and RTC peripherals are powered on.	8	μA
Hibernation	RTC memory is powered on. RTC peripherals are powered off.	7	μA
Power off	CHIP_PU is set to low level. The chip is powered off.	1	μA

5 Application Note

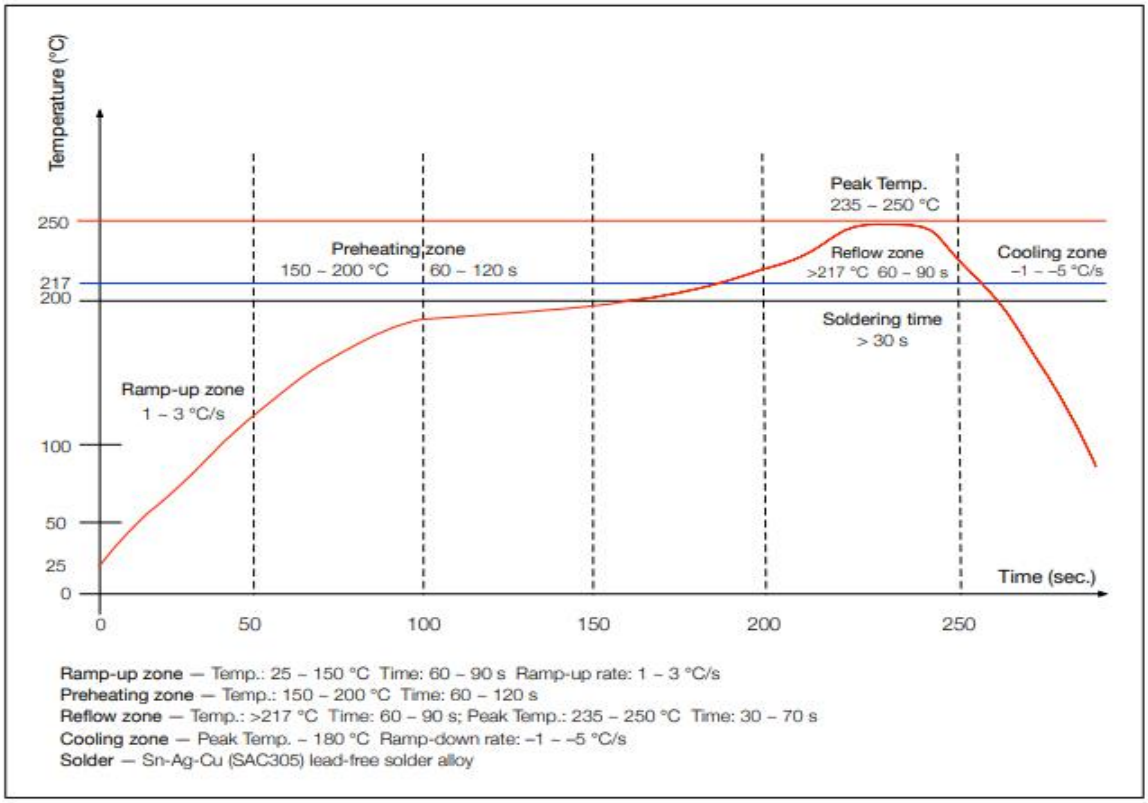
5.1 Module Dimensions

Figure 3 Module Dimensions



5.2 Reflow Profile

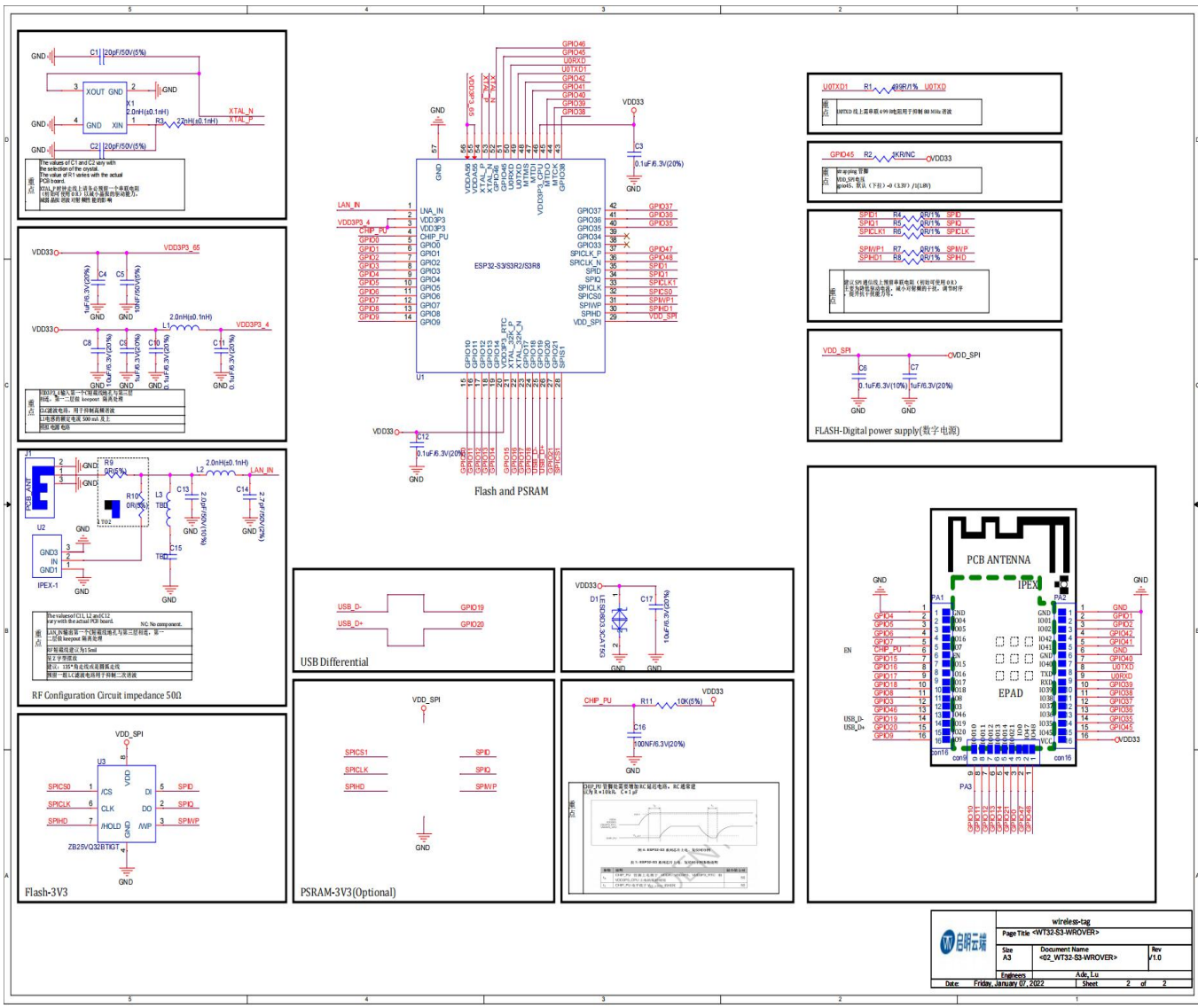
Figure 4 Reflow Profile



5.3 Peripheral Schematic

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

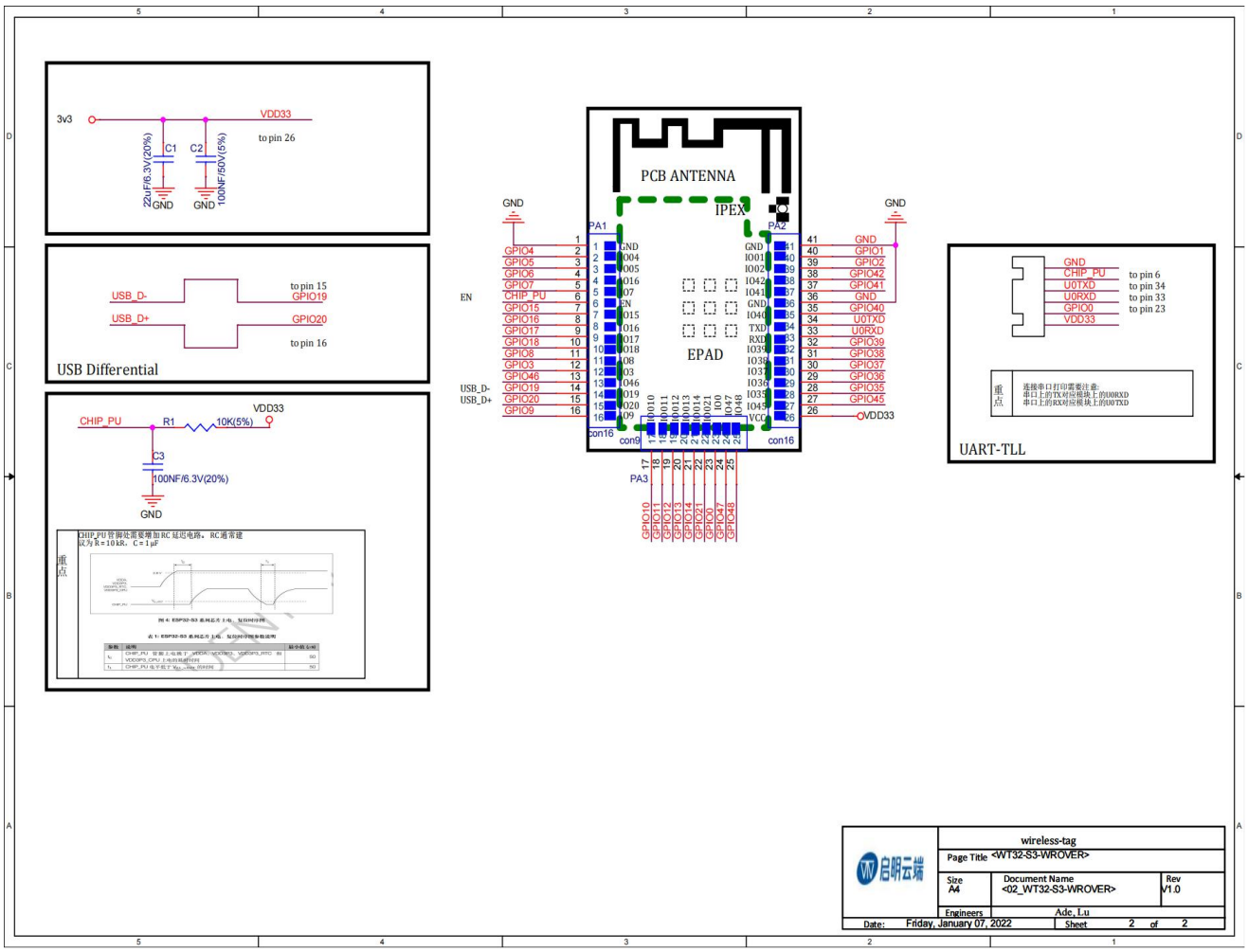
Figure 5 Module Schematics



5.4 Peripheral Design Schematic

The application circuit diagram of the connection between the module and peripheral devices (such as battery, antenna, reset button, JTAG interface, UART interface, etc.).

Figure 6 Application circuit diagram



6 Product Trial

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